Design Review 1:   
We created one block of an SRAM before design review 1. We chose the simplest devices because functionality was the only metric.   
  
1. Decoder

* The decoder is currently a parallel array of AND gates
* In the future, the decoder will include predecoders, correct sizing, possibly output buffers, an enable, and a model for the decoder

2. Word Lines

* The word lines will be modeled by an appropriate RC load (PI configuration?) and be hierarchical

3. Bitcells

* The bitcells are simple 6T bitcells with cell ratios and pull-up ratios defined by a simulation
* After a simulation, we will decide whether they should be LVT or HVT (to reduce leakage and therefore power)

4. Bitlines

* The bitlines will be modeled by an RC load determined from past research and simulations
* They may be hierarchical as well

5. MUXes

* The read and write MUXes are PMOS and NMOS pass gates, respectively, and need to be sized appropriately
* I'm not sure what the Block DeMUX and Block MUX should be... (-- Stevo)

6. Sense Amp

* The sense amp is currently a voltage latching sense amp, but future simulations should be done to pick an appropriate sense amp based on power and delay considerations

7. Write Amp

* The write amps are NMOSs right now

8. Precharge

* There are currently two precharge circuits
* The read precharge activates during every precharge cycle to charge up the bitlines
* The write precharge activates after a write to boost the charging time of the low bitline